REMARKS

The Examiner rejected claims 1-5, 8-11, 24-28, 32, 34-35, and 37-39 under 35 U.S.C. § 102(e) as being anticipated by the patent to Wilhelmsson. Applicant respectfully disagrees. In this response, Applicant has amended claim 1 to correct a minor informality not noted by the Examiner, and traverses the rejection.

The present invention relates to a self-calibrating Phase Lock Loop (PLL) that provides both a fast response during frequency acquisition, and a stable, substantially consistent output after locking. A typical PLL uses a loop filter to generate a smoothed control signal that ideally yields a low-noise/low-jitter oscillator output signal. The more heavily the control signal is filtered, the quieter the oscillator output signal is. However, heavy filtering undesirably increases the time it takes the PLL to "lock" to a new frequency. The present invention solves that problem by changing the loop filter to have less filtering when the PLL is unlocked, e.g., transitioning to a new frequency value, and more filtering when the PLL is locked. This loop filter adaptation is based on evaluating successive output values from the loop filter to determine whether the loop filter output is moving about some mean value, which would indicate a locked condition, or is trending up or down, for example, which would indicate an unlocked condition.

Claim 1 requires, "adapting a filter based on average control values determined from said successive control values." That is, the control logic of the present invention bases adjustments to the loop filter on the values of the loop filter output. The patent to Wilhelmsson, however, fails to teach this element. Wilhelmsson also discloses a PLL having a phase detector, a filter circuit, a DAC, a VCO, and a filter circuit controller to control the filter circuit. However, unlike the requirements of claim 1, the disclosed filter circuit controller does not control the loop filter based on the output of the filter circuit itself. Rather, it controls one or more filter circuit parameters as a *function of time*, and a decision on when to begin the

controlling the parameters. Importantly, the decision on when to begin control is irrespective of the values of the filter circuit output.

In more detail, Wilhelmsson looks at the rate of change of output values from the phase detector that serves as input to the filter circuit. If those values exhibit a high rate of change, Wilhelmsson deems the PLL to be unlocked. In response, a filter circuit controller changes one or more parameters of the filter circuit such that it has relatively less filtering (e.g., higher DC gain, higher frequency rolloff, etc.). This allows the filter circuit to enter saturation, and thus, facilitates fast acquisition of the new frequency. While the filter circuit is saturated, the filter circuit controller refrains from adjusting the filter circuit parameters. The filter circuit controller then monitors the output signal of the filter circuit to determine when the filter circuit reenters an unsaturated state, and then gradually changes the one or more filter circuit parameters according to a predetermined time schedule (see columns 9 and 10 of Wilhelmsson for an explicit discussion of this operation).

Notably, however, adjustments to the filter circuit parameters in Wilhelmsson are not "based on average control values determined from ... successive control values," as required by claim 1. In stark contrast, the adjustments are gradual and occur as a *function of time*. *See e.g., Wilhelmsson*, col. 11, ll. 1-12. In other words, the filter circuit of Wilhelmsson moves from a "light" filtering to a "heavy" filtering according to a timed schedule that is utterly independent of the filter circuit output. Apparently, the predetermined time of Wilhelmsson is known, or is assumed to be an appropriate time scale for moving from light to heavy loop filtering. Therefore, the patent to Wilhelmsson fails to anticipate claim 1 under § 102, and as such, Applicant respectfully requests the allowance of claim 1 and its dependent claims 2-9.

Regarding claims 10 and 24, they too contain language similar to that of claim 1. Specifically, claim 10 requires, "adapting a filter characteristic of said digital filter based on said average control values," and claim 24 requires, "control logic to control a filter characteristic of said loop filter based on an average control value determined from successive ones of said

control values to minimize clock deviations in said output signal." Thus, for the reasons stated above, Wilhelmsson fails to anticipate either of claims 10 or 24 under § 102. Accordingly, Applicant respectfully requests the allowance of claims 10 and 24, as well as their respective dependent claims 11-23 and 25-39.

Respectfully submitted,

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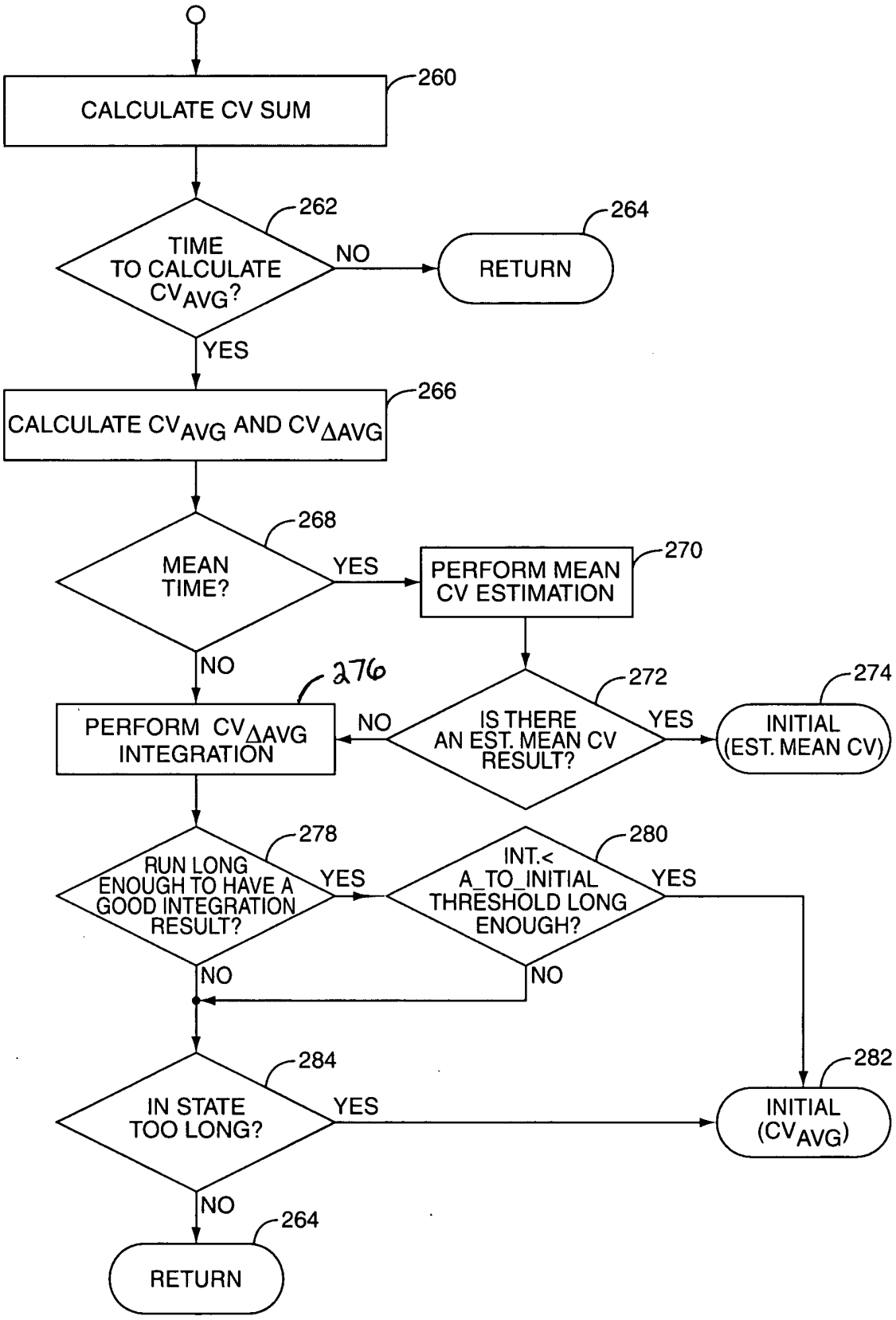

Approved.
T.W

FIG. 9

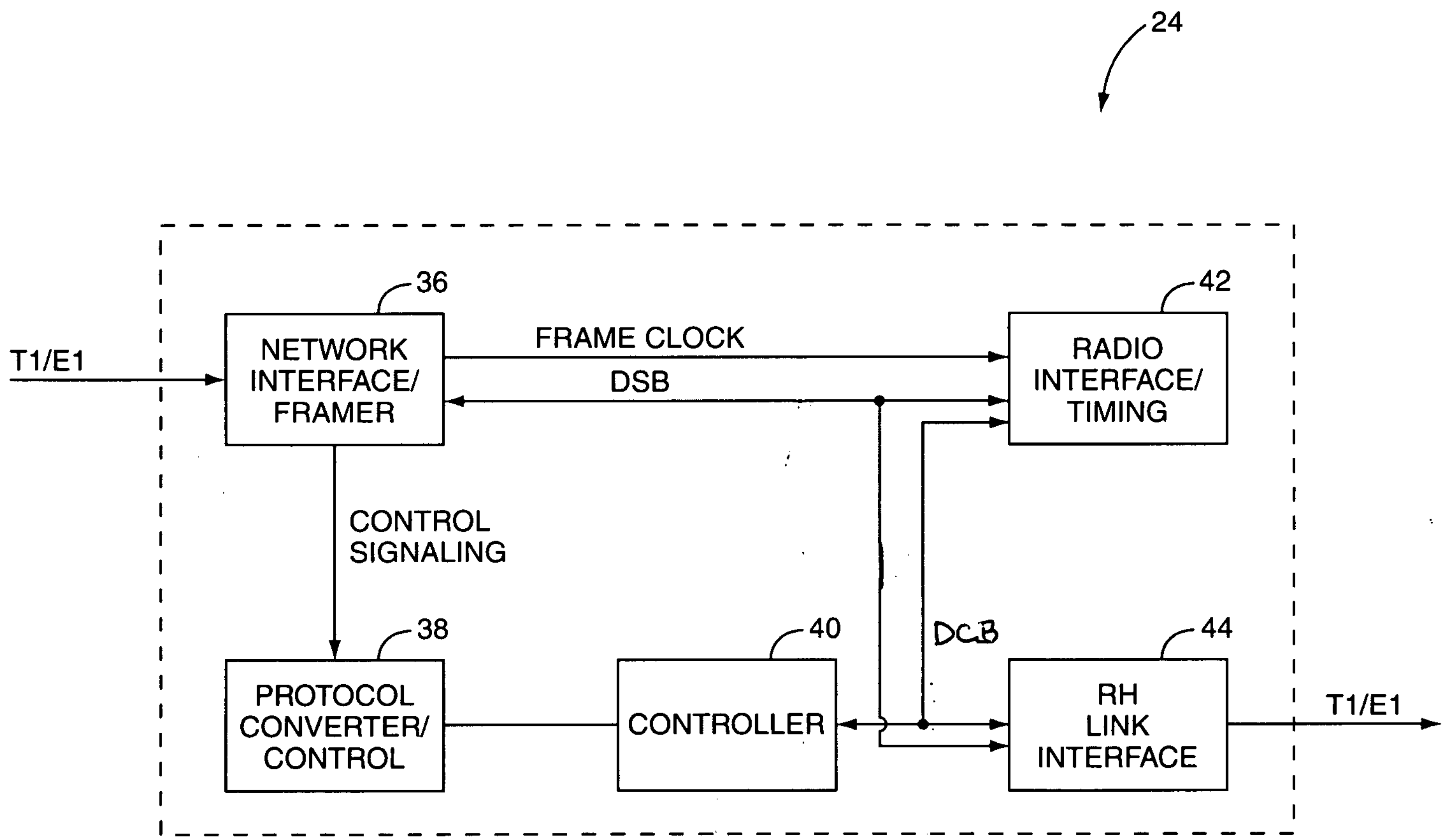

FIG. 2

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